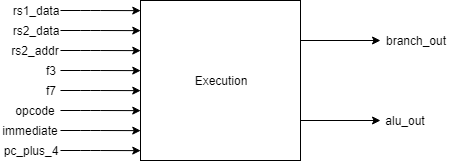
RISC-V EX

**RISC-V Execution Module**



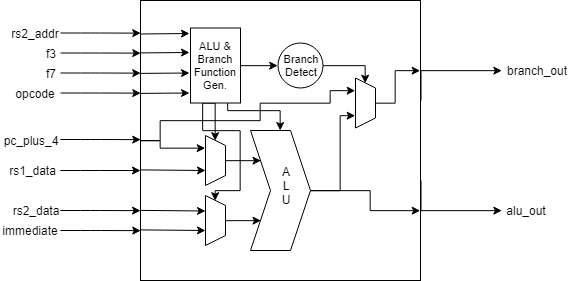
# Description

This is the RISC-V Processor’s execution module. This module performs the bulk of the work in the RISC-V processor. It receives the values retrieved from the registers selected by the current instruction, the “f3” and “f7” function codes, the current instruction opcode, the address of the second register as those bits in the instruction are sometimes encoded with shifting information, the immediate number generated in ID (Instruction Decode) and the next sequential value of the program counter. Based on what the current instruction is and what the function codes are, the EX will perform arithmetic, logical, shifting, comparisons and branch calculations. The EX will return the new branch address is there is a jump or a successful conditional jump, otherwise it will return the next sequential program counter value. It also returns the result of the ALU calculation that just took place.

# Data Dictionary

|  |  |
| --- | --- |
| **Signal Name** | **Description** |
| rs1\_data | Data retrieved from the first selected register |
| rs2\_data | Data retrieved from the second selected register |
| rs2\_addr | Address of second register operand, sometimes encoded with shifting information |
| f3 | RISC-V specific function code |
| f7 | RISC-V specific function code |
| opcode | Instruction identifier code |
| immediate | Immediate number encoded in instruction |
| pc\_plus\_4 | Next sequential program counter value |
| alu\_out | Output generated from ALU operation |
| branch\_out | Next address to be saved to the program counter |

# Implementation



The EX can be split into 2 parts. The ALU section and the Branch section. The “ALU & Branch Function Generation” process takes all the information about the current instruction, based on this information it generates signals to control the type of branch to be checked and what type of operation the ALU will complete. The two ALU input multiplexers are controlled by the “opcode” input, depending on the opcode they feed different inputs to the ALU. The output multiplexer selects between the next sequential program counter value and the result of the ALU operation depending on the success or failure of the branch detection unit.

# Revision History

* Revision 0.01 – Initial Revision, created document with block diagram, module description and data dictionary